Amendments to the Claims:

Following is a complete listing of the claims pending in the application, as amended:

1. (Original) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

depositing copper into recessed micro-structures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor workpiece with the deposited copper to an elevated temperature annealing process at a temperature below about 100 degrees Celsius for a time period that is sufficient to increase the grain size of the deposited copper.

2. (Canceled)

3. (Original) A method as claimed in Claim 1 wherein an electroplating waveform is used, at least in part, to ensure the sufficiently small copper grain size generation within the recessed microstructures.

4. (Original) A method as claimed in Claim 1 wherein an electroplating solution additive is used, at least in part, to ensure the sufficiently small copper grain size generation within the recessed microstructures.

5. (Canceled)

6. (Original) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

depositing copper into the recessed microstructures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor workpiece and the deposited copper to an elevated temperature annealing process at a temperature at or below about 250 degrees Celsius for a time period of no longer than 15 minutes, which time period is sufficient to increase the grain size of the deposited copper.

(Canceled)

8. (Original) A method as claimed in Claim 6 wherein an electroplating waveform is used, at least in part, to ensure the sufficiently small metal grain size.

9. (Original) A method as claimed in Claim 6 wherein an electroplating solution additive is used, at least in part, to ensure the sufficiently small metal grain size.

10. (Previously presented) A method for filling recessed microstructures at a surface of a semiconductor workpiece, the workpiece including at least one low-K dielectric layer, with copper metal comprising:

depositing copper into the recessed micro-structures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor workpiece with the deposited copper to an elevated temperature annealing process at a temperature selected to be below a predetermined temperature at which the low-K dielectric layer would suffer substantial degradation.

11. (Previously presented) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one low-K dielectric layer;

preparing a surface of the workpiece including the recessed microstructures with a metal seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer onto the surface of the workpiece using a process that generates copper grains that are sufficiently small to substantially fill the recessed microstructures;

annealing the electrochemically deposited copper for a predetermined period of time at an elevated temperature selected to be below a predetermined temperature at which the low-K dielectric layer would substantially degrade; and

removing copper metallization from the surface of the workpiece except from the recessed microstructures, after the annealing of the copper.

12. (Canceled)

13. (Original) A method as claimed in Claim 11 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and applying a metal seed layer over the barrier layer.

14. (Original) A method as claimed in Claim 13 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

15. (Original) A method as claimed in Claim 13 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

16. (Previously presented) A method as claimed in Claim 11 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a metal seed layer over the adhesion layer.

17. (Original) A method a claimed in Claim 11 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

18-23. (Canceled)

24. (Previously presented) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a seed layer for subsequent electrolytic copper deposition;

electrolytically depositing a copper layer onto the surface of the workpiece using an electrolytic process generating copper grains that are sufficiently small to substantially fill the recessed microstructures; and

subjecting the electrolytically deposited copper layer to an annealing process at a temperature at or below about 250 to 300 degrees Celsius to increase the copper grain size.

25. (Original) A method as claimed in Claim 24 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a seed layer over the adhesion layer.

26. (Original) A method as claimed in Claim 24 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

27. (Original) A method as claimed in Claim 26 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

28. (Original) A method as claimed in Claim 26 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

29. (Original) A method as claimed in Claim 24 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

30. (Previously presented) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one low-K dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a barrier layer for subsequent electrolytic copper deposition;

electrolytically depositing a copper layer to the surface of the workpiece using an electrolytic process that generates copper grains having a size sufficiently small to substantially fill the recessed microstructures; and

subjecting the electrolytically deposited copper layer to an annealing process at a temperature below which the low-K dielectric layer substantially degrades.

31. (Original) A method as claimed in Claim 30 wherein the annealing step takes place at a temperature corresponding to a baking temperature of the low-K dielectric.

32. (Previously presented) The method of Claim 1 wherein the temperature of the elevated temperature annealing process is between about 60 degrees Celsius and about 100 degrees Celsius.

33. (Previously presented) The method of Claim 1 wherein the surface of the semiconductor workpiece is subjected to the elevated temperature annealing process for no longer than 15 minutes.

34. (Previously presented) The method of Claim 1 wherein the surface of the semiconductor workpiece is subjected to the elevated temperature annealing process for less than one minute.

35. (Previously presented) The method of Claim 11 wherein the predetermined temperature is at or below about 300 degrees Celsius.

36. (Previously presented) The method of Claim 11 wherein the predetermined temperature is at or below about 250 degrees Celsius.

37. (Previously presented) The method of Claim 11 wherein the predetermined temperature is at or below about 100 degrees Celsius.

38. (Previously presented) The method of Claim 11 wherein the predetermined temperature is between about 60 degrees Celsius and about 100 degrees Celsius.

39. (Previously presented) The method of Claim 11 wherein the workpiece is subjected to the elevated temperature annealing for no longer than 15 minutes.

40. (Previously presented) The method of Claim 11 wherein the workpiece is subjected to the elevated temperature annealing for less than one minute.

41. (Previously presented) The method of Claim 1 wherein depositing the copper comprises contacting the surface of the workpiece with a copper-containing electroplating solution and applying electroplating power.

42. (Previously presented) The method of Claim 41 wherein the electroplating power is initially applied at a first current for a predetermined first period of time, then applied at a higher second current for a predetermined second period of time.

43. (Previously presented) The method of Claim 41 wherein the surface of the workpiece is contacted with the electroplating solution for a predetermined dwell period before the electroplating power is applied.

44. (Previously presented) The method of Claim 41 wherein the electroplating power is applied as a direct current.

45. (Previously presented) The method of Claim 41 wherein the electroplating power is applied as a forward pulsed waveform at a frequency of between 1 and 1000 Hz.

46. (Previously presented) The method of Claim 45 wherein the frequency is between 5 and 20 Hz with a duty cycle of at least 50 percent.

47. (Previously presented) The method of Claim 41 wherein the workpiece is spun while electroplating power is applied.

48. (Previously presented) The method of Claim 1 wherein the copper is deposited via electroplating for a period of time sufficient to deposit excess copper which extends above the surface of the workpiece.

49. (Previously presented) The method of Claim 48 further comprising removing the excess copper after the workpiece is subjected to the elevated temperature annealing.

50. (Previously presented) The method of Claim 49 wherein the excess copper is removed via chemical mechanical polishing.

51. (Previously presented) A method of processing a semiconductor workpiece having a surface including a sub-micron recessed microstructure, comprising:

depositing a conductive seed layer in the recessed microstructure;

thereafter, electroplating copper to substantially fill the recessed microstructure and to deposit excess copper which extends above the surface of the workpiece;

thereafter, thermally treating the electroplated copper at a temperature of about 60 degrees Celsius to about 100 degrees Celsius for no longer than 15 minutes, thereby reducing resistivity of the copper; and

thereafter, removing the excess copper.

52. (Previously presented) The method of Claim 51 wherein the excess copper is removed via chemical mechanical polishing.

53. (Previously presented) The method of Claim 51 wherein an electroplating waveform is used, at least in part, to ensure sufficiently small grain size in the electroplated copper to substantially fill the recessed microstructure.

54. (Previously presented) The method of Claim 51 wherein an electroplating solution additive is used, at least in part, to ensure sufficiently small grain size in the electroplated copper to substantially fill the recessed microstructure.

55. (Previously presented) The method of Claim 51 wherein the recessed microstructure is defined, at least in part, as a recess in a dielectric layer, the method further comprising applying a barrier over the dielectric layer before depositing the seed layer.

56. (Previously presented) The method of Claim 55 wherein the seed layer is deposited on the barrier layer using a physical vapor deposition process.

57. (Previously presented) A method of treating a semiconductor workpiece having a base having a surface, a dielectric layer carried on the surface of the base, and recessed sub-micron structures formed in the dielectric layer, comprising:

depositing a conductive seed layer on the dielectric layer and in the recessed sub-micron structures;

contacting the seed layer with a copper-containing electroplating solution;

after a predetermined dwell time, applying electroplating power to the seed layer to electrolytically deposit copper metal from the electroplating solution to substantially fill the recessed sub-micron structures and to deposit excess copper metal which extends above a surface of the dielectric layer; then

reducing resistivity of the electrolytically deposited copper metal by subjecting the workpiece to an elevated temperature annealing process at a temperature that is at or below about 250 degrees Celsius.

58. (Previously presented) The method of Claim 57 wherein the annealing process is carried out at a temperature that is at or below about 100 degrees Celsius.

59. (Previously presented) The method of Claim 57 wherein the annealing process is carried out at a temperature that is between about 60 degrees Celsius and about 100 degrees Celsius.

60. (Previously presented) The method of Claim 57 wherein the workpiece is subjected to the annealing process for no longer than 15 minutes.

61. (Previously presented) The method of Claim 57 wherein the workpiece is subjected to the annealing process for less than one minute.

62. (Previously presented) The method of Claim 57 wherein the resistivity is reduced by greater than 10% in the elevated temperature annealing process.

63. (Previously presented) The method of Claim 57 further comprising depositing a barrier layer on the dielectric layer and in the sub-micron structures prior to depositing the seed layer.

64. (Previously presented) The method of Claim 57 wherein the electroplating power is initially applied at a first current for a predetermined first period of time, then applied at a higher second current for a predetermined second period of time.

65. (Previously presented) The method of Claim 57 wherein the electroplating power is applied as a direct current.

66. (Previously presented) The method of Claim 57 wherein the electroplating power is applied as a forward pulsed waveform at a frequency of between 1 and 1000 Hz.

67. (Previously presented) The method of Claim 66 wherein the frequency is between 5 and 20 Hz with a duty cycle of at least 50 percent.

68. (Previously presented) The method of Claim 57 wherein the workpiece is spun while electroplating power is applied.

69. (Previously presented) The method of Claim 57 further comprising removing the excess copper after the workpiece is subjected to the elevated temperature annealing process.

70. (Previously presented) A method of treating a semiconductor workpiece having a base having a surface, a dielectric layer carried on the surface of the base, and recessed sub-micron structures formed in the dielectric layer, comprising:

depositing a conductive seed layer on the dielectric layer and in the recessed sub-micron structures;

contacting the seed layer with a copper-containing electroplating solution;

applying electroplating power to the seed layer a first power level for a predetermined first period of time, then applying electroplating power to the seed layer a higher second power level for a time sufficient to electrolytically substantially fill the recessed sub-micron structures with copper metal and to deposit excess copper metal which extends above a surface of the dielectric layer; then

reducing resistivity of the electrolytically deposited copper metal by subjecting the workpiece to an elevated temperature annealing process at a temperature that is at or below about 250 degrees Celsius.

71. (Previously presented) The method of Claim 70 wherein the annealing process is carried out at a temperature that is at or below about 100 degrees Celsius.

72. (Previously presented) The method of Claim 70 wherein the annealing process is carried out at a temperature that is between about 60 degrees Celsius and about 100 degrees Celsius.

73. (Previously presented) The method of Claim 70 wherein the workpiece is subjected to the annealing process for no longer than 15 minutes.

74. (Previously presented) The method of Claim 70 wherein the workpiece is subjected to the annealing process for less than one minute.

75. (Previously presented) The method of Claim 70 wherein the resistivity is reduced by greater than 10% in the elevated temperature annealing process.

76. (Previously presented) The method of Claim 70 further comprising depositing a barrier layer on the dielectric layer and in the sub-micron structures prior to depositing the seed layer.

77. (Previously presented) The method of Claim 70 wherein the seed layer is contacted with the electroplating solution for a predetermined dwell period before the electroplating power is applied.

78. (Previously presented) The method of Claim 70 wherein the electroplating power is applied as a direct current.

79. (Previously presented) The method of Claim 70 wherein the electroplating power is applied at the second power level as a forward pulsed waveform at a frequency of between 1 and 1000 Hz.

80. (Previously presented) The method of Claim 79 wherein the frequency is between 5 and 20 Hz with a duty cycle of at least 50 percent.

81. (Previously presented) The method of Claim 70 wherein the workpiece is spun while electroplating power is applied.

82. (Previously presented) The method of Claim 70 further comprising removing the excess copper after the workpiece is subjected to the elevated temperature annealing process.

83. (Previously presented) A method of treating a semiconductor workpiece having a base having a surface, a dielectric layer carried on the surface of the base, and recessed sub-micron structures formed in the dielectric layer, comprising:

depositing a conductive seed layer on the dielectric layer and in the recessed sub-micron structures;

contacting the seed layer with a copper-containing electroplating solution;

applying electroplating power to the seed layer in a forward pulsed waveform at a frequency of between 1 and 1000 Hz to electrolytically substantially fill the recessed sub-micron structures with copper metal and to deposit excess copper metal which extends above a surface of the dielectric layer; then

reducing resistivity of the electrolytically deposited copper metal by subjecting the workpiece to an elevated temperature annealing process at a temperature that is at or below about 250 degrees Celsius.

84. (Previously presented) The method of Claim 83 wherein the frequency is between 5 and 20 Hz with a duty cycle of at least 50 percent.

85. (Previously presented) The method of Claim 83 wherein the forward pulsed waveform has a duty cycle of 50-95 percent.

86. (Previously presented) The method of Claim 83 wherein the annealing process is carried out at a temperature that is at or below about 100 degrees Celsius.

87. (Previously presented) The method of Claim 83 wherein the annealing process is carried out at a temperature that is between about 60 degrees Celsius and about 100 degrees Celsius.

88. (Previously presented) The method of Claim 83 wherein the workpiece is subjected to the annealing process for no longer than 15 minutes.

89. (Previously presented) The method of Claim 83 wherein the workpiece is subjected to the annealing process for less than one minute.

90. (Previously presented) The method of Claim 83 wherein the resistivity is reduced by greater than 10% in the elevated temperature annealing process.

91. (Previously presented) The method of Claim 83 further comprising depositing a barrier layer on the dielectric layer and in the sub-micron structures prior to depositing the seed layer.

92. (Previously presented) The method of Claim 83 wherein the seed layer is contacted with the electroplating solution for a predetermined dwell period before the electroplating power is applied.

93. (Previously presented) The method of Claim 83 wherein the electroplating power is initially applied at a first current for a predetermined first period of time, then applied at a higher second current for a predetermined second period of time, the second current comprising the forward pulsed waveform.

94. (Previously presented) The method of Claim 83 wherein the workpiece is spun while electroplating power is applied.

95. (Previously presented) The method of Claim 83 further comprising removing the excess copper after the workpiece is subjected to the elevated temperature annealing process.